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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,542	06/27/2003	Akihisa Shimomura	0756-7171	6138
31780	7590	10/05/2005	EXAMINER	
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			ISAAC, STANETTA D	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EJL

Office Action Summary	Application No. 10/607,542	Applicant(s) SHIMOMURA ET AL.	
	Examiner Stanetta D. Isaac	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) 2, 4, 6, 8, 10, 12, 25 and, 27 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,7,9,11,13-24,26 and 28-43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the amendment filed on 7/05/05. Currently, claims 1-43 are pending.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 7, 9, 11, 13, 14, 15-24, 26 and 28-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al., US Patent 6165,876.

Yamazaki discloses the semiconductor method as claimed. See figures 1A-12C, and corresponding text, where Yamazaki teaches, pertaining to claims 1 and 3, a method of manufacturing a semiconductor device, comprising: forming a crystalline semiconductor layer 105 by heating an amorphous semiconductor layer 103 over a substrate that has an insulating surface 102 (after adding a metal element for accelerating crystallization thereto, pertaining to

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claim 3) (figure 2A; col. 14, lines 50-67); introducing an impurity of one conductivity type into the crystalline semiconductor layer (figure 2B; col. 15, lines 1-9); irradiating the crystalline semiconductor layer with laser light to redistribute the impurity (figure 2B; col. 15, lines 1-9); removing a surface portion of the crystalline semiconductor layer after the irradiation (figure 2C; col. 15, lines 20-30); and forming a channel portion of an insulated gate field effect transistor from a remaining portion of the crystalline semiconductor layer, wherein the remaining portion comprises the impurity (figure 2D; col. 15, lines 20-30).

Pertaining to claims 5 and 7, Yamazaki teaches, wherein a source of the laser light is one selected from a continuous wave YAG, laser, YVO₄ laser, YLF laser, and YAlO₃ laser (col. 9, lines 44-50).

Pertaining to claims 9 and 11, Yamazaki teaches, wherein 40 nm or more of the thickness of the surface portion is removed (figure 2C; col. 15, lines 1-20).

Pertaining to claims 24 and 26, Yamazaki teaches, wherein a concentration of the impurity element in the crystalline semiconductor layer is 1×10^{15} to $5 \times 10^{18}/\text{cm}^3$ and in the range of the concentration being $\pm 10\%$ for an average (col. 15, lines 1-9).

Pertaining to claims 38 and 39, Yamazaki teaches, wherein the impurity element comprises boron (col. 15, lines 1-9).

Pertaining to claims 13 and 19, Yamazaki teaches, a method of manufacturing a semiconductor device, comprising: forming an amorphous semiconductor layer having a thickness of 60 nm or more (figure 2A; col. 14, lines 50-67); crystallizing the amorphous semiconductor layer to obtain a crystalline semiconductor layer (figure 2A; col. 14, lines 50-67); introducing an impurity element into the crystalline semiconductor layer by acceleration voltage

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30kV or less (figure 2A; col. 14, lines 50-67); irradiating the crystalline semiconductor layer with laser light after introducing the impurity element whereby the impurity element redistributed (figure 2B; col. 15, lines 1-9); and removing a surface portion of the crystalline semiconductor layer, after the irradiating (figure 2C; col. 15, lines 20-30), wherein the crystalline semiconductor layer after the removing comprises the impurity element (figure 2D; col. 15, lines 20-30).

Pertaining to claim 14, Yamazaki teaches, wherein a method for crystallizing the amorphous semiconductor layer is selected from one of furnace annealing, radiant heat method, gas heat method and rapid thermal annealing (col. 14, lines 59-67).

Pertaining to claims 15 and 20, Yamazaki teaches, wherein a source of the laser light is one selected from a continuous wave YAG, laser, YVO₄ laser, YLF laser, and YAlO₃ laser (col. 9, lines 44-50).

Pertaining to claims 16 and 21, Yamazaki teaches, wherein a thickness of the surface portion of the crystalline semiconductor layer removed is 10 nm to 50 nm (figure 2C; col. 15, lines 1-20).

Pertaining to claims 17 and 22, Yamazaki teaches, further comprising: patterning the crystalline semiconductor layer to form an island shape (figure 2C).

Pertaining to claims 18 and 23, Yamazaki teaches, wherein a concentration of the impurity element in the crystalline semiconductor layer is 1×10^{15} to $5 \times 10^{18}/\text{cm}^3$ and in the range of the concentration being $\pm 10\%$ for an average (col. 15, lines 1-9).

Pertaining to claims 40 and 41, Yamazaki teaches, wherein the impurity element comprises boron (col. 15, lines 1-9).

Pertaining to claims 28 and 29, Yamazaki teaches, a method of manufacturing a semiconductor device, comprising: forming an amorphous semiconductor layer over a substrate that has an insulating surface (figure 2A; col. 14, lines 50-67); crystallizing the amorphous semiconductor layer by heat to obtain a crystalline semiconductor layer (figure 2A; col. 14, lines 50-67); introducing an impurity element into the amorphous semiconductor layer by accelerating the impurity element with the acceleration voltage 30kV or less (figure 2A; col. 14, lines 50-67); irradiating the crystalline semiconductor layer with laser light after introducing the impurity element whereby the impurity element is redistributed (figure 2B; col. 15, lines 1-9); removing a surface portion of the crystalline semiconductor layer after the removing comprises the impurity element (figure 2D; col. 15, lines 20-30).

Pertaining to claims 30 and 34, Yamazaki teaches, wherein a source of the laser light is one selected from a continuous wave YAG, laser, YVO₄ laser, YLF laser, and YAlO₃ laser (col. 9, lines 44-50).

Pertaining to claims 31 and 35, Yamazaki teaches, wherein a thickness of the surface portion of the crystalline semiconductor layer removed is 10 nm to 50 nm (figure 2C; col. 15, lines 1-20).

Pertaining to claims 32 and 36, Yamazaki teaches, further comprising: patterning the crystalline semiconductor layer to form an island shape (figure 2C).

Pertaining to claims 33 and 37, Yamazaki teaches, wherein a concentration of the impurity element in the crystalline semiconductor layer is 1×10^{15} to $5 \times 10^{18}/\text{cm}^3$ and in the range of the concentration being $\pm 10\%$ for an average (col. 15, lines 1-9).

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Pertaining to claims 42 and 43, Yamazaki teaches, wherein the impurity element comprises boron (col. 15, lines 1-9).

Response to Arguments

Applicant's arguments with respect to claims 1, 3, 5, 7, 9, 11, 13-24, 26 and 28-37 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
October 2, 2005



MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER